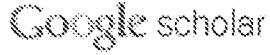


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(interleave OR stripe OR alternate) (flash) odd Advanced Scholar Search

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Did you mean: (interleave OR stripe OR alternate) (flash) **hdd** ("lba" OR block)

A.3.3.V.50MHz synchronous 16Mb **flash** memory

D Mills, M Bauer, A Bashir... - Solid-State Circuits ..., 1995 - ieeexplore.ieee.org

... The addresses are sequential, and therefore **alternate** banks. ... Strip 0 Even Bank [Strip 1 **Odd** Bank ... Page 3. Figure 6 Regenerative feedback repeater test chip micrograph TA 7.1: A 3.3V 50MHz Synchronous 16Mb **Flash** Memory (Continued from page 121) ...

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Flash memory control method and information processing system therewith

T Tobita, J Kitahara, T Tsunehiro... - US Patent ..., 1996 - Google Patents

... 25,1996 [54] **FLASH** MEMORY CONTROL METHOD AND INFORMATION PROCESSING SYSTEM

THEREWITH [75] Inventors: Tsunehiro Tobita; Jun Kitahara, both of Yokohama; Takashi Tsunehiro,

Ebina; Kunihiro Katayama, Yokohama; Ryuichi Hattori, Kawasaki; Yukihiro ...

Cited by 122 - Related articles - [All 2 versions](#)

Flash memory card including plural **flash** memories and circuitry for selectively outputting

ready/busy signals in different operating modes

KB Robinson, RD Eslick, MA Levy... - US Patent ..., 1995 - Google Patents

... D. Verner, "Designing an Updatable BIOS Using **Flash** Memory," 7997 Memory Handbook, Intel Corporation, pp. ... Sheet 3 of 33 5,388,248 JOS D15 08 X16 X8 HIGH BYTE **ODD** BYTE D7 D0

LOW BYTE EVEN BYTE I44i **BLOCK** PAIR HIGH/ODD-ZONE **BLOCK** I47 — I41 ...

Cited by 87 - Related articles - [All 2 versions](#)

PROGRAMMING A **FLASH** MEMORY DEVICE

S Arikome - US Patent App. 12/973,11G, 2010 - Google Patents

... This embodiment shows that the **odd** and even page verify voltage levels are the same starting at page 0 but by page 62 and 63, the verify voltages are different. ... **Alternate** embodiments may include the **flash** memory cell of the present invention in other types of ...

[All 2 versions](#)

MEMORY BLOCK REALLOCATION IN A **FLASH** MEMORY DEVICE

J Han... - US Patent App. 20,090/244,982, 2009 - freepatentsonline.com

... For example, all the **odd** pages from one **block** can be allocated to another **block** or blocks ... a **block** diagram of one embodiment of a circuit for reallocating pages of a NAND **flash** **block**. ... If an **alternate** embodiment divides the **block** into more than two physical blocks, the 32 global ...

Cashed

NAND **flash** memory and data programming method thereof

H Maejima - US Patent 7,400,634, 2008 - Google Patents

... A Double-Level Vth Select Gate Array Archi- tecture for Multi-Level NAND **Flash** Memories", Symposium ... Unselected="VPASS' H" CELSRC for EVEN Worst case:Bit data[01010-]or[1010V-■](**Alternate**) FIG. ... 12 550 16 .J CELSRC for **ODD**-**Block** N 17 .J •**Block** N+1 18 .J CELSRC ...

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MEMORY BLOCK REALLOCATION IN A **FLASH** MEMORY DEVICE

JM Han... - US Patent App. 12/478,377, 2009 - Google Patents

... If an **alternate** embodiment divides the **block** into more than two physical blocks, the 32 global wordlines ... Therefore, over the lifespan of the **flash** memory, physical **block** 0 is accessed less than half of ... The memory device of claim 3 wherein the x pages are **odd** pages and the y ...

Apparatus and architecture for a compact **flash** memory controller

F Pieu... - US Patent 6,778,436, 2004 - Google Patents

... In another embodiment, an **alternate** allows data stored in the **flash** memory to be transmitted via a number of specified input devices. 11 Claims, 4 Drawing Sheets 200 203 Page 2. US Patent Aug. ... **Flash** memory module 222a store the **odd** data seg- ment of a received ...

Cited by 12 - Related articles - [All 3 versions](#)

Flash memory card with all zones chip enable circuitry

RD Eslick, DM Brown, LC Pao, BL Dipt... - US Patent ..., 1995 - Google Patents

... One **flash** memory card has addressable circuitry for selectively causing first, second, and third **flash** memories to operate in an active mode ... Sheet 3 of 33 D15 D8 D7 DO X16 HIGH BYTE LOW BYTE X8 **ODD** BYTE EVEN BYTE HIGH/ODD-ZONE **BLOCK** 147 141 16 ...

Cited by 31 - Related articles - [All 2 versions](#)

[PDF] from fasteststorage.com

[PDF] **Flash** in the Enterprise

J Bowen - Texas Memory Systems White Paper, 2007 - fasteststorage.com

... At first it may seem **odd** that rewritable media would be considered "read only," but when you examine how EEPROMs work, the reason that "ROM" remains becomes clear. ... In addition, a RAID-5 layout is used across the **Flash** modules with a 16 KB **stripe** width to allow ...

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